Amendments to the Claims:

Please amend Claims 9, 14, 16, and 19 and add new claims 23-30 as noted in the listing below. This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-8 previously canceled.

9. (previously amended) An apparatus, comprising:

a storage structure to store at least one entry, the at least one entry to include a register identifier value;

a first physical rename register of a first length; and

a second physical rename register of a second length different than the first length, wherein the first and second rename registers are distinct from each other and do not share any common bits;

a logical predicate register; and

rename logic to map an instance of the logical predicate register to a selected physical rename register, where the selected physical rename register is selected from a plurality of registers comprising the first physical rename register and the second physical rename register;

wherein the register identifier value is to indicate a current length, wherein the current length is selected from a set including the first length and the second length;

wherein the logical register includes a plurality of x bit positions;

wherein a selected one of the x bit positions may be accessed individually responsive to a first instruction that indicates the selected bit position;

wherein all x bit positions may be accessed together responsive to a second instruction; and

the rename logic is further to allocate the first physical rename register responsive to the first instruction, the rename logic further to allocate the second physical rename register responsive to the second instruction.

10. (previously amended) The apparatus of claim 9, wherein:

a subset including y of the x bits may be accessed responsive to a third instruction, where $y > 1$; and

the rename logic is further to allocate the first physical rename register responsive to the third instruction.

11. (original) The apparatus of claim 10, wherein:

the length of the first physical rename register includes y bit positions.

12. (original) The apparatus of claim 11, wherein:

the entry is further to include a position identifier, the position identifier to indicate a selected one of the y bit positions of the first physical rename register.

13. (original) The apparatus of claim 12, wherein:

the selected one of the y bit positions of the first physical rename register corresponds to the selected bit position indicated by the first instruction.

14. (currently amended) A method comprising:

determining that a current instruction indicates as a destination register a multiple-bit-field (MBF) predicate register having n bit positions, where n > 1; and

allocating a physical rename register for the destination register;

wherein allocating further comprises allocating a physical rename register of a first length responsive to the current instruction indicating a partial-bit write of only 1 bit position of the MBF predicate register and further comprises allocating a physical rename register of a second length responsive to the current instruction indicating a bulk-bit write of x bit positions of the predicate register, where x is greater than 1 and x is less than or equal to n.

15. (original) The method of claim 14, wherein:

allocating further comprises modifying a rename map table to indicate the allocated physical rename register.

16. (currently amended) The method of claim 14, wherein:

the allocating further includes allocating a physical rename register of the first length responsive to the current instruction indicating a partial-bit write of y bit positions of the predicate register, where $1 < y < x$.

17. (previously amended) The method of claim 16, wherein:

the y bit positions are contiguous.

18. (original) The method of claim 14, wherein:

the x bit positions are contiguous.

19. (currently amended) The method of claim 14, wherein:

the allocating further comprises allocating a physical rename register of the second length responsive to the current instruction indicating a bulk-bit write of all n bit positions of the predicate register.

20. (original) The method of claim 16, wherein:

y=2.

21. (original) The method of claim 16, wherein:

y=4.

22. (original) The method of claim 14, further comprising:

modifying the current instruction to indicate the allocated physical rename register in place of the MBF register.

23. (New) An apparatus comprising:

a storage structure to store at least one entry, the at least one entry to include a register type identifier value;

a first physical rename register of a first type, the first type having a first length; and

a second physical rename register of a second type, the second type having a second length different than the first length; and

rename logic to map an instance of a logical predicate register to a selected one of the physical rename registers dependent upon the number of bits of the logical predicate register that are to be written by a current instruction, the rename logic further to place a register type

identifier value into the storage structure entry to indicate the type of the selected physical rename register.

24. (New) The apparatus of claim 23, wherein:

the first and second physical_rename registers belong to a plurality of t physical rename registers, wherein $t > 2$.

25. (New) The apparatus of claim 23, wherein:

the storage structure is to store a plurality of entries, each of the plurality of entries to include a corresponding register type identifier value.

26. (New) The apparatus of claim 23, wherein:

the first physical rename register is one of a plurality (z) of physical rename registers of the first length.

27. (New) The apparatus of claim 23, wherein:

the second physical rename register is one of a plurality (m) of physical rename registers of the second length.

28. (New) The apparatus of claim 26, wherein:

the second physical rename register is one of a plurality (m) of physical rename registers of the second length.